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POST-CLEANING CHAMBER SEASONING METHOD

Field of the Invention

[001]The present invention relates to chemical vapor deposition (CVD) technology used in the deposition of material layers such as polysilicon in the fabrication of integrated circuits on a semiconductor wafer substrate. More particularly, the present invention relates to a novel post-cleaning seasoning method for the seasoning of a CVD chamber in order to reduce the quantity of residual particles remaining in the chamber.

Background of the Invention

[002]The fabrication of various solid state devices requires the use of planar substrates, or semiconductor wafers, on which integrated circuits are fabricated. The final number, or yield, of functional integrated circuits on a wafer at the end of the IC fabrication process is of utmost importance to semiconductor manufacturers, and increasing the yield of circuits on the wafer is the main goal of semiconductor fabrication. After packaging, the circuits on the wafers are tested, wherein non-functional dies are marked using an inking process and the functional dies on the wafer are separated and sold. IC fabricators increase the yield of dies on a wafer by exploiting economies of scale. Over 1000 dies may be formed on a single wafer which measures from six

to twelve inches in diameter.

[003]Various processing steps are used to fabricate integrated circuits on a semiconductor wafer. These steps include sequential deposition of conductive and insulative layers on the silicon wafer substrate; formation of a photoresist or other mask such as titanium oxide or silicon oxide, in the form of the desired metal interconnection pattern, using standard lithographic or photolithographic techniques; subjecting the wafer substrate to a dry etching process to remove material from one or more conducting layers from the areas not covered by the mask, thereby etching the conducting layer or layers in the form of the masked pattern on the substrate; removing or stripping the mask layer from the substrate typically using reactive plasma and chlorine gas, thereby exposing the top surface of the conductive interconnect layer; and cooling and drying the wafer substrate by applying water and nitrogen gas to the wafer substrate.

[004]The numerous processing steps outlined above are used to cumulatively apply multiple electrically conductive and insulative layers on the wafer and pattern the layers to form the circuits. Additional techniques, such as dual damascene processes, are used to form conductive vias which establish electrical contact between vertically-spaced conductive lines or

layers in the circuits. The finished semiconductor product includes microelectronic devices including transistors, capacitors and resistors that form the integrated circuits on each of multiple die on a single wafer.

[005]In the semiconductor industry, CMOS (complementary metal-oxide semiconductor) technology is extensively used in the fabrication of IC devices. CMOS technology typically involves the use of overlying layers of semiconductor material with the bottom layer being a dielectric layer and the top layer being a layer of doped silicon material that serves as a low- resistivity electrical contact gate electrode. The gate electrode, also referred to as a gate stack, typically overlies the dielectric layer.

[006] In the semiconductor fabrication industry, silicon oxide (SiO_2) is frequently used for its insulating properties as a gate oxide or dielectric. As the dimensions of device circuits on substrates become increasingly smaller, the gate dielectric thickness must decrease proportionately in field effect transistors (FETs) to approximately 3 to 3.5 nonometers. Accordingly, device performance and reliability can be adversely affected by such factors as interfacial defects, defect precursors and diffusion of dopants through gate dielectrics, as

well as unintended variations in thickness in the gate oxide layer among central and peripheral regions of the layer.

[007]Two types of CMOS device structures which are commonly fabricated in semiconductor technology include the MOSCAP (metal oxide semiconductor capacitor) structure and the MOSFET (metal oxide semiconductor field effect transistor) structure. Both of these structures include a substrate on which is deposited a dielectric layer having a high dielectric constant (k), such as a pad oxide layer. A silicon-containing gate, or gate stack, is deposited on the dielectric layer and connects a pair of trench oxide layers (in the case of a MOSCAP structure) or source and drain regions (in the case of a MOSFET structure).

[008]One gate stack fabrication technique involves the deposition of polycrystalline silicon (polysilicon) on the high-k dielectric layers of multiple substrates simultaneously in a vertical process furnace to form the gate stack on each substrate. Such a deposition process requires a relatively high thermal budget (620 degrees C at a process time of typically about 1.5 hours). Another technique involves the deposition of amorphous silicon on the dielectric layer in a process furnace to form the gate stack on each of the multiple substrates. Compared to the polysilicon deposition process, the deposition of amorphous silicon has a

lower thermal budget (550 degrees C at a process time of typically about 2 hours). Therefore, due to the relatively lower thermal budget of the amorphous silicon deposition process in the furnace processing of multiple substrates, amorphous silicon has a higher stability than polysilicon when deposited as a gate stack on a dielectric layer having a high dielectric constant.

[009]Formation of a gate stack on a pad oxide layer in fabrication of both the MOSCAP and MOSFET structures is currently carried out typically on single substrates using chemical vapor deposition (CVD) in a CVD process chamber. In the fabrication of MOSCAP and MOSFET structures, polysilicon or amorphous silicon is deposited on a high-k dielectric layer in a CVD process chamber. Polysilicon is deposited on the dielectric layer at a temperature of typically about 675 degrees C for a process time of about 1 minutes. Amorphous silicon, on the other hand, is deposited on the dielectric layer at a temperature of typically about 575 degrees C for about 10 min. This is accomplished by reacting hafnium dioxide (HfO_2) with silicon (Si) to form silicon oxides (SiOx), according to the following equation:

$$HfO_2 + Si \text{ --}\Delta\text{--> } HfO_2\text{-}x + SiOx$$

[0010] Ideally, the silicon oxides are deposited in an even layer over the high-k dielectric layer to form the high-stability

gate stack structure. However, it has been found that in spite of the lower thermal budget of the amorphous silicon deposition process, the amorphous silicon is less stable than the polysilicon in single-wafer processing applications due to unintended chemical reactions between the hafnium dioxide and cleaning agent used to clean the process chamber.

[0011] During gate stack fabrication or other extended use of the CVD chamber in semiconductor fabrication, some of the silicon oxide or other high molecular weight residues accumulate on the interior surfaces of the process chamber. Because these residues are loosely attached to the chamber wall interior surfaces, the residues have a tendency to break off and contaminate device structures being fabricated on the wafer. Accordingly, at regular intervals, the CVD process chamber must be subjected to a chamber-cleaning procedure to remove the residues of silicon oxides from the interior chamber walls.

[0012] To prevent accumulation of excessive quantities of residues inside a CVD chamber, the chamber is dry-cleaned after a predetermined period of operation such that micro-particles attached to the interior sidewalls of the chamber are removed. After longer periods of operation, preventative maintenance (PM) of the chamber is carried out to restore the reaction chamber to

ideal operating conditions.

[0013] Even after regular dry-cleaning and PM cleanings of the CVD chamber are carried out, some residual particles frequently remain attached to the interior surfaces of the chamber. Accordingly, a novel chamber seasoning method is needed to provide a seasoning film on the interior surfaces of a CVD chamber in order to minimize the accumulation of residual particles in the chamber during chemical vapor deposition processes.

[0014] An object of the present invention is to provide a novel method for the seasoning of a process chamber in such a manner as to enhance the quality of device features fabricated on substrates in the chamber.

[0015] Another object of the present invention is to provide a novel chamber seasoning method which includes providing a seasoning film on the interior surfaces of a process chamber to prevent the excessive accumulation of particles in the chamber.

[0016] Still another object of the present invention is to provide a novel chamber cleaning method which is particularly adapted for a CVD chamber but may be adapted to a variety of

process chambers for a variety of semiconductor fabrication or other processes.

[0017] Yet another object of the present invention is to provide a novel chamber cleaning method which improves the stability of films deposited on a substrate.

[0018] A still further object of the present invention is to provide a novel chamber seasoning method which may be carried out after a chamber-cleaning process and includes deposition of an oxygen-rich seasoning film on the interior surfaces of a CVD chamber.

[0019] Another object of the present invention is to provide a novel chamber seasoning method which is effective in reducing the quantity of defects in devices fabricated on a wafer and increasing the WAT (wafer acceptance testing) yield.

Summary of the Invention

[0020] In accordance with these and other objects and advantages, the present invention is generally directed to a novel method for seasoning a process chamber in such a manner that the quantity of particulate residues remaining in the chamber after semiconductor fabrication or other processes are

carried out in the chamber, is substantially reduced. The seasoning method includes providing a seasoning film on the interior surfaces of a process chamber, typically after cleaning of the chamber. Accordingly, the quantity of particulate by-product residues which remain in the chamber after processing is substantially reduced.

[0021] According to a typical embodiment of the invention, the seasoning film formed on the interior surfaces of the process chamber is a silicon dioxide (SiO_2) film. The seasoning film may be formed on the chamber walls by introducing a silicon-containing gas such as silane (SiH_4), and an oxygen-containing precursor gas such as molecular oxygen (O_2), into the chamber and reacting the silicon-containing gas with the oxygen-containing precursor gas to form the silicon dioxide seasoning film on the interior surfaces of the chamber. Other oxygen-containing precursor gases which are suitable for carrying out the present invention include N_2O, NO and CO_2, for example.

[0022] In another embodiment, dichlorosilane ($SiCl_2H_2$) gas is reacted with ammonia (NH_3) to form a silicon nitride seasoning film on the interior surfaces of the chamber. In still another embodiment, trimethylsilane [$Si(CH_3)_3H$] is used as the silicon precursor source gas for deposition of a silicon carbide

seasoning film on the interior chamber surfaces.

Brief Description of the Drawings

[0023] The invention will now be described, by way of example, with reference to the accompanying drawings, in which:

[0024] Figure 1 is a schematic of a CVD process chamber in implementation of the method of the present invention;

[0025] Figure 1A is an enlarged sectional view, taken along section line 1A in Figure 1, of a portion of a CVD process chamber wall and a seasoning film provided on the inner surface of the wall according to the method of the present invention; and

[0026] Figure 2 is a process flow diagram which illustrates a typical process flow in implementation of the method of the present invention.

Detailed Description of the Invention

[0027] The present invention has particularly beneficial utility in the seasoning of chemical vapor deposition (CVD) chambers used to form material layers in semiconductor fabrication, such as to deposit a silicon-containing layer on a high-k dielectric layer in the fabrication of gate stack structures on semiconductor wafer substrates, for example.

However, the invention is not so limited in application and is equally applicable to semiconductor IC fabrication processes in general as well as other industrial processes.

[0028] The present invention contemplates a method which includes providing a seasoning film of high oxygen content on the interior surfaces of a process chamber, particularly a CVD chamber. The seasoning film reduces the quantity of residual process particles which remain in the chamber after chemical vapor deposition processes are carried out in the chamber. This reduces the quantity of contaminating particles which are available to contaminate layers deposited on substrates in subsequent processes. Consequently, the incidence of defects in device features fabricated on substrates is substantially decreased, thereby promoting the WAT (wafer acceptance testing) yield.

[0029] The seasoning film is typically a silicon dioxide (SiO_2) layer which may be deposited on the interior surfaces of the chamber by reacting a silicon-containing gas with an oxygen-containing precursor gas in the chamber. Preferably, the seasoning film is formed on the interior chamber surfaces after a chamber cleaning process is carried out.

[0030] In one embodiment according to the method of the present invention, a silicon dioxide (SiO_2) seasoning film is formed on the interior surfaces of the process chamber by reacting silane (SiH_4) gas with molecular oxygen (O_2). Alternatively, the silicon dioxide seasoning film is formed by reacting silane with nitrous oxide (N_2O), nitric oxide (NO), carbon dioxide (CO_2)or any other suitable oxygen-containing precursor gas.

[0031] In another embodiment, dichlorosilane ($SiCl_2H_2$) gas is reacted with ammonia (NH_3) to form a silicon nitride (Si_3N_4) seasoning film on the interior surfaces of the chamber. In still another embodiment, trimethylsilane [$Si(CH_3)_3H$] is used as the silicon precursor source gas and carbon dioxide (CO_2) is used as the carbon precursor gas for deposition of a silicon carbide (SiC) seasoning film on the interior chamber surfaces.

[0032] In the various embodiments, the seasoning film may have a thickness of typically from about 2 μm to about 20 μm on the interior surfaces of a process chamber. Preferably, the seasoning film has a thickness of typically at least about 10 μm.

[0033] Typical process conditions for formation of the seasoning film are as follows: chamber temperature (about 500 to about 700 degrees C); chamber pressure (about 10 Torr to about

760 Torr, or 1 atmosphere); and process time (about 0.5 min. to about 10 min.).

[0034] Referring to Figure 1, a typical CVD process chamber 10 suitable for implementation of the method of the present invention is shown. The chamber 10 includes a chamber wall 12 that defines a chamber interior 13. A gas distribution plate or "showerhead" 14 is provided in the top of the chamber 10 for the introduction of process gases from a gas panel 16 into the chamber interior 13, by actuation of a control unit 18. A vacuum pump 20 is provided in gas communication with the chamber interior 13 for the evacuation of gases therefrom. A pedestal support 23, on which is provided a pedestal 22 for supporting a substrate 24, is upward-standing in the chamber interior 13.

[0035] The chamber 10 may be further equipped with temperature control features used to control the temperature of the pedestal 22 and substrate 24 resting thereon, as is known by those skilled in the art. The showerhead 14 and the pedestal 22 also form a pair of spaced-apart electrodes. When an electric field is generated between the electrodes, the process gases introduced into the chamber 10 are ignited into a plasma.

[0036] Typically, the electric field is generated by connecting the pedestal 22 to a source of radio frequency (RF)

power (not shown) through a matching network (not shown). Alternatively, the RF power source and matching network may be coupled to the showerhead 14 or to both the showerhead 14 and the pedestal 22. Optionally, a remote plasma source 26 may be provided in communication with the chamber interior 13 to provide a remotely-generated plasma to the chamber interior 13, typically through a chamber inlet 28 that extends into the chamber interior 13.

[0037] In typical operation of the CVD process chamber 10 to deposit a material layer or layers on a substrate 24, the substrate 24 is initially placed on the pedestal 22. Deposition gases are introduced into the chamber interior 13 through the showerhead 14 and ignited to form a plasma which contacts the substrate 24 to deposit material layers thereon. In the fabrication of gate stack structures which are characteristic of MOSCAP (metal oxide semiconductor capacitor) structures and MOSFET (metal oxide semiconductor field effect transistor) structures, for example, amorphous silicon or polysilicon is deposited on a high-k dielectric material layer.

[0038] During the deposition process, silicon or other material residues become deposited on the interior surfaces, including those of the chamber wall 12, of the chamber 10.

Typically, these silicon residues are removed by introducing etchant HCl or other etchant cleaning gas into the chamber interior 13 through the showerhead 14, such that the HCl or other etchant cleaning gas contacts the interior surfaces of the chamber 10 and removes the silicon residues from those surfaces to eliminate or minimize the risk of contaminating devices that are subsequently fabricated on substrates 24. However, the HCl or other etchant cleaning gas is typically incapable of removing all of the silicon or other material residues from the interior surfaces of the chamber 10.

[0039] Referring to Figures 1, 1A and 2, in accordance with the method of the present invention, a seasoning film 30 is deposited on the interior surfaces of the process chamber 10, as follows. First, the chamber 10 is cleaned such as by using HCl or other etchant gas, as indicated in step 1 of Figure 2 and according to the knowledge of those skilled in the art. Next, as indicated in step 2 of Figure 2, the chamber 10 is initially set to the proper chamber temperature and pressure necessary for the layer-seasoning process. In typical application, the chamber 10 is set at a temperature of typically from about 500 degrees C to about 700 degrees C and a pressure of typically from about 10 Torr to about 760 Torr, or 1 atmosphere.

[0040] Next, as shown in step 3, the seasoning film precursor gases are introduced into the chamber interior 13, typically through the showerhead 14. In one embodiment, in which the seasoning film 30 is silicon dioxide (SiO_2), the silicon precursor gas is silane (SiH_4) and the oxygen precursor gas is O_2, N_2O, NO, CO_2 or other suitable oxygen-containing precursor gas. In another embodiment, in which the repellent coating layer 30 is silicon nitride (Si_3N_4), the silicon precursor gas is dichlorosilane ($SiCl_2H_2$) and the nitrogen precursor gas is ammonia (NH_3). In still another embodiment, in which the repellent coating layer 30 is silicon carbide (SiC), the silicon precursor gas is trimethylsilane [$Si(CH_3)_3H$] and the carbon precursor gas is carbon dioxide (CO_2).

[0041] The seasoning film precursor gases remain in the chamber interior 13 for a period of from typically about 0.5 min. to about 10 min., during which time the silicon dioxide, silicon nitride or silicon carbide coats the interior surfaces, including the chamber walls 12 and the showerhead 14, as the seasoning film 30. As shown in Figure 1A, the seasoning film 30 preferably has a thickness 31 of typically from about 2 μm to about 10 μm.

[0042] As indicated in step 4 of Figure 2, after the seasoning film 30 has been deposited on the interior surfaces of the

chamber 10, layer-forming precursor gases and by-products which remain in the chamber 10 are evacuated therefrom typically by operation of the vacuum pump 20. Accordingly, the chamber 10 is seasoned or primed for CVD processing of substrates 24 therein, and a substrate 24 is placed on the pedestal 22, as shown in step 5, for processing, as shown in step 6. After completion of the CVD process, the substrate 24 is removed from the chamber 10, as shown in step 7.

[0043] During the CVD deposition process of step 5, the seasoning film 30 repels the formation of amorphous silicon and other material residues on the interior surfaces of the chamber 10. Therefore, after competion of the CVD deposition process, these residues are readily evacuated from the chamber 10 with the remaining process gases using the vacuum pump 20.

[0044] While the preferred embodiments of the invention have been described above, it will be recognized and understood that various modifications can be made in the invention and the appended claims are intended to cover all such modifications which may fall within the spirit and scope of the invention.